Abstract

A digital bus includes a transmitter unit, a receiver unit, and a transmission medium to couple the transmitter unit to the receiver unit and to provide a path for exchanging information between the transmitter unit and the receiver unit. The receiver unit includes a first-in-first-out (FIFO) unit and a synchronizer unit for receiving information from the transmitter unit. The synchronizer unit receives a plurality of write clock signals and a reset signal and generates a read reset signal positioned with respect to the plurality write clock signals and a sample clock signal. The read reset signal has a latency with respect to each of the plurality of write reset signals of between 0 and 1 clock cycles.